Electronic Version
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Claims

[c1] 1. A low power consumption oscillation circuit, the oscillation circuit activating an initial oscillation operation according to an enable signal, and operating according to a high working voltage and a low working voltage, comprising:

an enable circuit, outputting an initial oscillation signal after the initial oscillation operation according a feedback control signal;

an oscillator delay circuit, coupled to the enable circuit, receiving the initial oscillation signal from the enable circuit and alternately generating a high level oscillation signal oscillating in a high voltage area and a low level oscillation signal oscillating in a low voltage area according the initial oscillation signal, wherein the high voltage area is between the high working voltage and a low-limit voltage higher than the low working voltage, and the low voltage area is between the low working voltage and an up-limit voltage lower than the high working voltage; and

a feedback control network, coupled to the oscillator delay circuit, integrating the high level oscillation signal and the low level oscillation signal as the feedback con-

trol signal and outputting the feedback control signal to the enable circuit.

[c2] 2. The low power consumption oscillation circuit of claim 1, wherein the initial oscillation signal outputted from the enable circuit comprises two partial signals separately oscillating in the high voltage area and low voltage area.

[c3] 3. The low power consumption oscillation circuit of claim 2, wherein the enable circuit comprises:
a P-type semiconductor device combination, coupled to the high working voltage, outputting the high level oscillation signal according to the feedback control signal;
an N-type semiconductor device combination, coupled to the low working voltage, outputting the high level oscillation signal according to the feedback control signal; and
a loading device, coupled to the P-type semiconductor device combination and N-type semiconductor device combination and disposed between the P-type semiconductor device combination and N-type semiconductor device combination.

[c4] 4. The low power consumption oscillation circuit of claim 2, wherein the oscillator delay circuit comprises a delay circuit.

[c5] 5. The low power consumption oscillation circuit of claim 4, wherein the delay circuit comprises:
a pull-up device coupled to the high working voltage, receiving the high level oscillation signal outputted from the enable circuit;
a pull-down device coupled to the low working voltage, receiving the low level oscillation signal outputted from the enable circuit;
a loading device, coupled to the pull-up and pull-down devices and disposed between the pull-up and pull-down devices;
a first output terminal, coupled to the pull-up device and the loading device and disposed between the pull-up device and the loading device, outputting the high level oscillation signal to the feedback control network; and
a second output terminal, coupled to the pull-down device and the loading device and disposed between the pull-down device and the loading device, outputting the low level oscillation signal to the feedback control network.

[c6] 6. The low power consumption oscillation circuit of claim 2, wherein the oscillation delay circuit comprises a plurality of delay circuits.

[c7] 7. The low power consumption oscillation circuit of claim

6, wherein the delay circuits comprise:
a first delay circuit, coupled to the enable circuit; and
a plurality of backend delay circuits, the backend delay circuits comprising delay circuits connected in series, wherein a second delay circuit is coupled to the first delay circuit, and an output delay circuit is coupled to the feedback control network.

[c8] 8. The low power consumption oscillation circuit of claim 7, wherein the first delay circuit comprises:
a pull-up device, coupled to the high working voltage, receiving the high level oscillation signal outputted from the enable circuit;
a pull-down device, coupled to the low working voltage, receiving the low level oscillation signal outputted from the enable circuit;
a loading device, coupled to the pull-up and pull-down devices and disposed between the pull-up and pull-down devices;
a first output terminal, coupled to the pull-up device and the loading device and disposed between the pull-up device and the loading device, outputting the high level oscillation signal to the feedback control network; and
a second output terminal, coupled to the pull-down device and the loading device and disposed between the pull-down device and the loading device, outputting the

low level oscillation signal to the feedback control network.

[c9] 9. The low power consumption oscillation circuit of claim 7, wherein the delay circuits comprise:
a pull-up device, coupled to the high working voltage, receiving the high level oscillation signal outputted from a front end of the pull-up device;
a pull-down device, coupled to the low working voltage, receiving the low level oscillation signal outputted from a front end of the pull-down device;
a loading device, coupled to the pull-up and pull-down devices and disposed between the pull-up and pull-down devices;
a first output terminal, coupled to the pull-up device and the loading device and disposed between the pull-up device and the loading device, outputting the high level oscillation signal to a backend of the pull-up device; and
a second output terminal, coupled to the pull-down device and the loading device and disposed between the pull-down device and the loading device, outputting the low level oscillation signal to the pull-down device.

[c10] 10. The low power consumption oscillation circuit of claim 6, wherein the feedback control network comprises a plurality of inverters, the inverters comprising:
a plurality of inverters, each of the inverters comprising

a P-type semiconductor device and an N-type semiconductor device; and

a plurality of external control inverters, each of the external control inverters comprising a P-type semiconductor device, an N-type semiconductor device, an external P-type semiconductor device and an external N-type semiconductor device, wherein each of the inverters and each of the external control inverters are alternately coupled to each other in series.

[c11] 11. The low power consumption oscillation circuit of claim 10, wherein the external control inverters comprise:

the external P-type semiconductor device, coupled to the high working voltage and the P-type semiconductor device and disposed between the high working voltage and the P-type semiconductor device, receiving the high level oscillation signal outputted from an even delay circuit counted backward; and

the external N-type semiconductor device, coupled to the low working voltage and the N-type semiconductor device and disposed between the low working voltage and the N-type semiconductor device, receiving the low level oscillation signal outputted from the even delay circuit counted backward.

[c12] 12. The low power consumption oscillation circuit of claim 1, wherein the oscillator delay circuit comprises a delay circuit.

[c13] 13. The low power consumption oscillation circuit of claim 12, wherein the delay circuit comprises:
a pull-up device, coupled to the high working voltage, receiving the initial oscillation signal;
a pull-down device, coupled to the low working voltage, receiving the initial oscillation signal;
a loading device, coupled to the pull-up and pull-down devices and disposed between the pull-up and pull-down devices;
a first output terminal, coupled to the pull-up device and the loading device and between the pull-up device and the loading device, outputting the high level oscillation signal; and
a second output terminal, coupled to the pull-down device and the loading device and disposed between the pull-down device and the loading device, outputting the low level oscillation signal.

[c14] 14. The low power consumption oscillation circuit of claim 1, wherein the oscillation delay circuit comprises a plurality of delay circuits.

[c15] 15. The low power consumption oscillation circuit of

claim 14, wherein the delay circuits comprise:
a first delay circuit, coupled to the enable circuit; and
a plurality of backend delay circuits, the backend delay circuits comprising delay circuits connected in series, wherein a second delay circuit is coupled to the first delay circuit, and an output delay circuit is coupled to the feedback control network.

[c16] 16. The low power consumption oscillation circuit of claim 15, wherein the first delay circuit comprises:
a pull-up device, coupled to the high working voltage, receiving the initial oscillation signal;
a pull-down device, coupled to the low working voltage, receiving the initial oscillation signal;
a loading device, coupled to the pull-up and pull-down devices and disposed between the pull-up and pull-down devices;
a first output terminal, coupled to the pull-up device and the loading device and disposed between the pull-up device and the loading device, outputting the high level oscillation signal to the second delay circuit; and
a second output terminal, coupled to the pull-down device and the loading device and disposed between the pull-down device and the loading device, outputting the low level oscillation signal to the second delay circuit.

[c17] 17. The low power consumption oscillation circuit of claim 15, wherein the delay circuits comprise:
a pull-up device, coupled to the high working voltage, receiving the high level oscillation signal outputted from a front end of the pull-up device;
a pull-down device, coupled to the low working voltage, receiving the low level oscillation signal outputted from a front end of the pull-down device;
a loading device, coupled to the pull-up and pull-down devices and disposed between the pull-up and pull-down devices;
a first output terminal, coupled to the pull-up device and the loading device and disposed between the pull-up device and the loading device, outputting the high level oscillation signal; and
a second output terminal, coupled to the pull-down device and the loading device and disposed between the pull-down device and the loading device, outputting the low level oscillation signal.

[c18] 18. The low power consumption oscillation circuit of claim 14, wherein the feedback control network comprises a plurality of inverters and a plurality of external control inverters, and each of the inverters and each of the external control inverters are alternately coupled to each other in series.

[c19] 19. The low power consumption oscillation circuit of claim 18, wherein the external control inverters comprise:

an inverter, comprising a P-type semiconductor device and an N-type semiconductor device coupled in series;

an external P-type semiconductor device, coupled to the high working voltage and the P-type semiconductor device and disposed between the high working voltage and the P-type semiconductor device, receiving the high level oscillation signal outputted from an even delay circuit counted backward; and

an external N-type semiconductor device, coupled to the low working voltage and the N-type semiconductor device and disposed between the low working voltage and the N-type semiconductor device, receiving the low level oscillation signal outputted from the even delay circuit counted backward.

[c20] 20. A delay circuit of a low power consumption oscillation circuit, operating according to a high working voltage and a low working voltage, comprising:

a pull-up device, coupled to the high working voltage, receiving a first signal;

a pull-down device, coupled to the low working voltage, receiving a second signal;

a loading device, coupled to the pull-up and the pull-

down devices and disposed between the pull-up and the pull-down devices;

a first output terminal, coupled to the pull-up device and the loading device and disposed between the pull-up device and the loading device, outputting a signal oscillating in a high voltage area; and

a second output terminal, coupled to the pull-down device and the loading device and disposed between the pull-down device and the loading device, outputting a signal oscillating in a low voltage area, wherein the high voltage area is between the high working voltage and a low-limit voltage higher than the low working voltage, and the low voltage area is between the low working voltage and an up-limit voltage lower than the high working voltage.

[c21] 21. The delay circuit of a low power consumption oscillation circuit of claim 20, wherein the first signal is as same as the second signal.

[c22] 22. The delay circuit of a low power consumption oscillation circuit of claim 20, wherein the pull-up device comprises a P-type semiconductor device.

[c23] 23. The delay circuit of a low power consumption oscillation circuit of claim 20, wherein the pull-down device comprises an N-type semiconductor device.

[c24] 24. The delay circuit of a low power consumption oscillation circuit of claim 20, wherein the loading device comprises an active device.

[c25] 25. The delay circuit of a low power consumption oscillation circuit of claim 1, wherein the feedback control network comprises an inverter.

[c26] 26. The delay circuit of a low power consumption oscillation circuit of claim 25, wherein the inverter comprises a P-type semiconductor device and an N-type semiconductor which are coupled in series.